

LCFC confidential

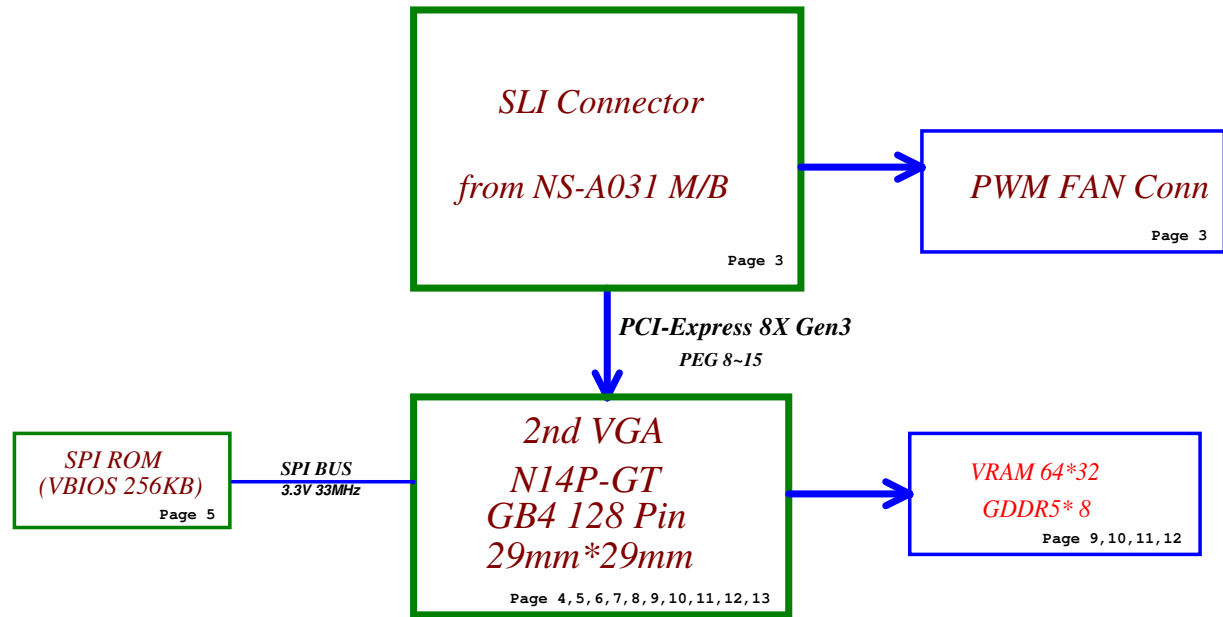
Schematics Document

NS-A031 ODD to VGA board schematic

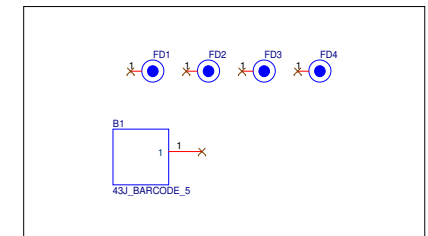
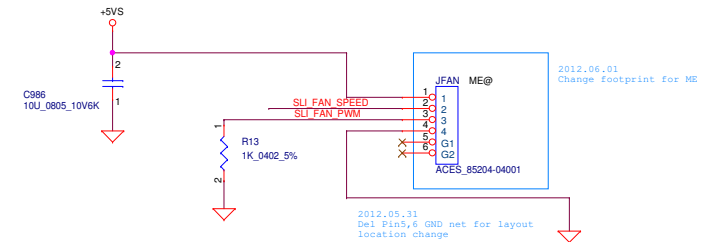
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REV:1.0

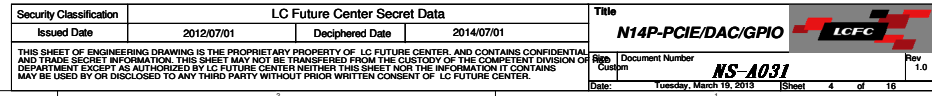
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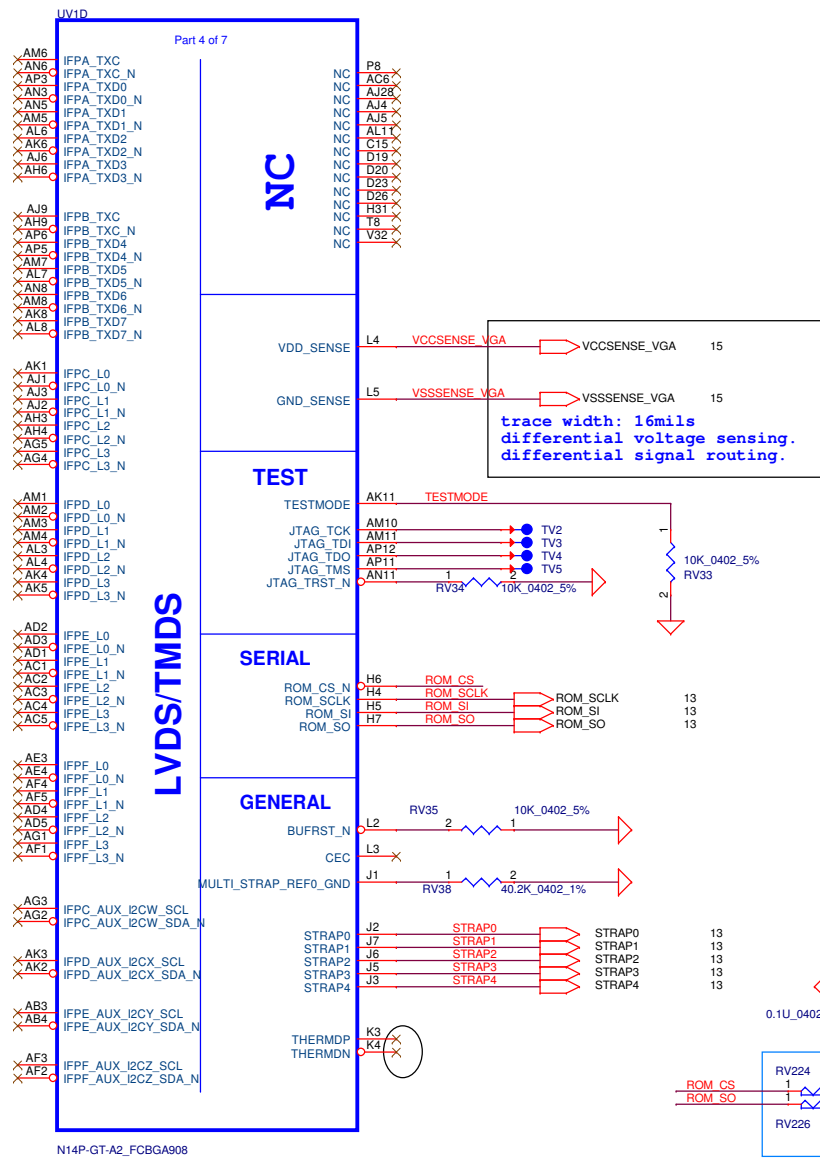


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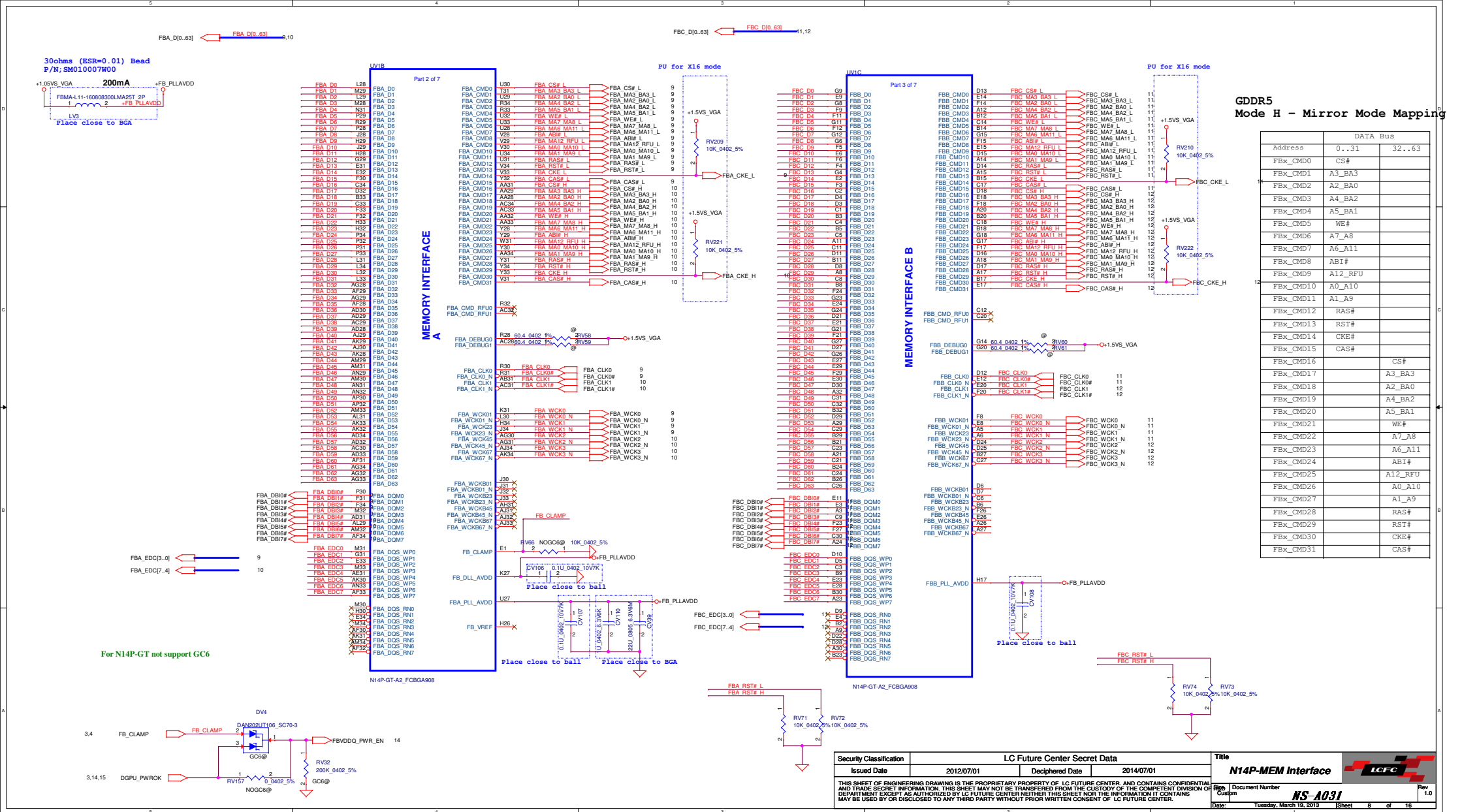
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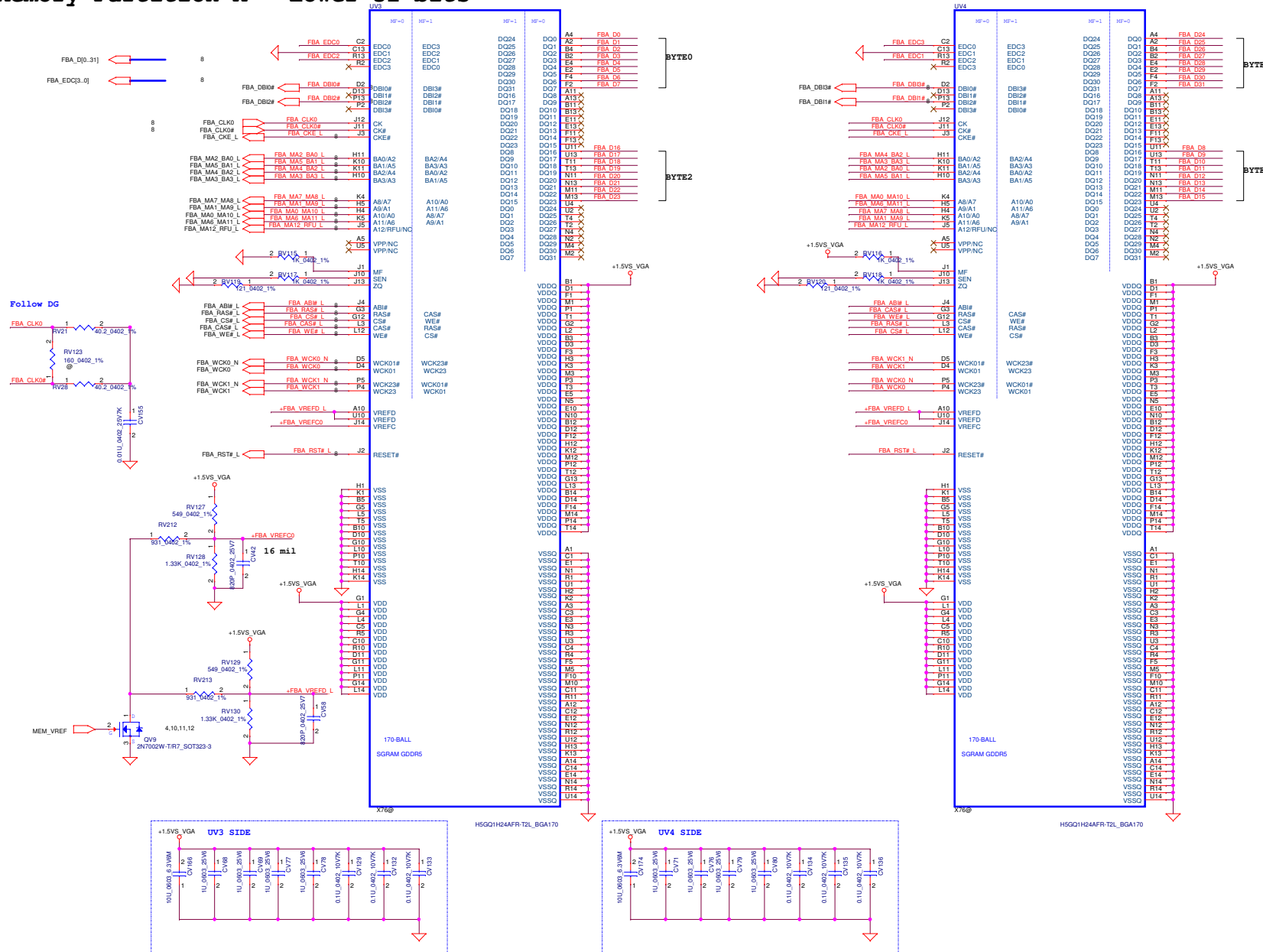


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		DATA Bus	
Address	0..31	32..63	
FBx_CMD0	CS#		
FBx_CMD1	A3_BA3		
FBx_CMD2	A2_BA0		
FBx_CMD3	A4_BA2		
FBx_CMD4	A5_BA1		
FBx_CMD5	WE#		
FBx_CMD6	A7_A8		
FBx_CMD7	A6_A11		
FBx_CMD8	AB1#		
FBx_CMD9	A12_RFU		
FBx_CMD10	A0_A10		
FBx_CMD11	A1_A9		
FBx_CMD12	RAS#		
FBx_CMD13	RST#		
FBx_CMD14	CKE#		
FBx_CMD15	CAS#		
FBx_CMD16		CS#	
FBx_CMD17		A3_BA3	
FBx_CMD18		A2_BA0	
FBx_CMD19		A4_BA2	
FBx_CMD20		A5_BA1	
FBx_CMD21		WE#	
FBx_CMD22		A7_A8	
FBx_CMD23		A6_A11	
FBx_CMD24		AB1#	
FBx_CMD25		A12_RFU	
FBx_CMD26		A0_A10	
FBx_CMD27		A1_A9	
FBx_CMD28		RAS#	
FBx_CMD29		RST#	
FBx_CMD30		CKE#	
FBx_CMD31		CAS#	

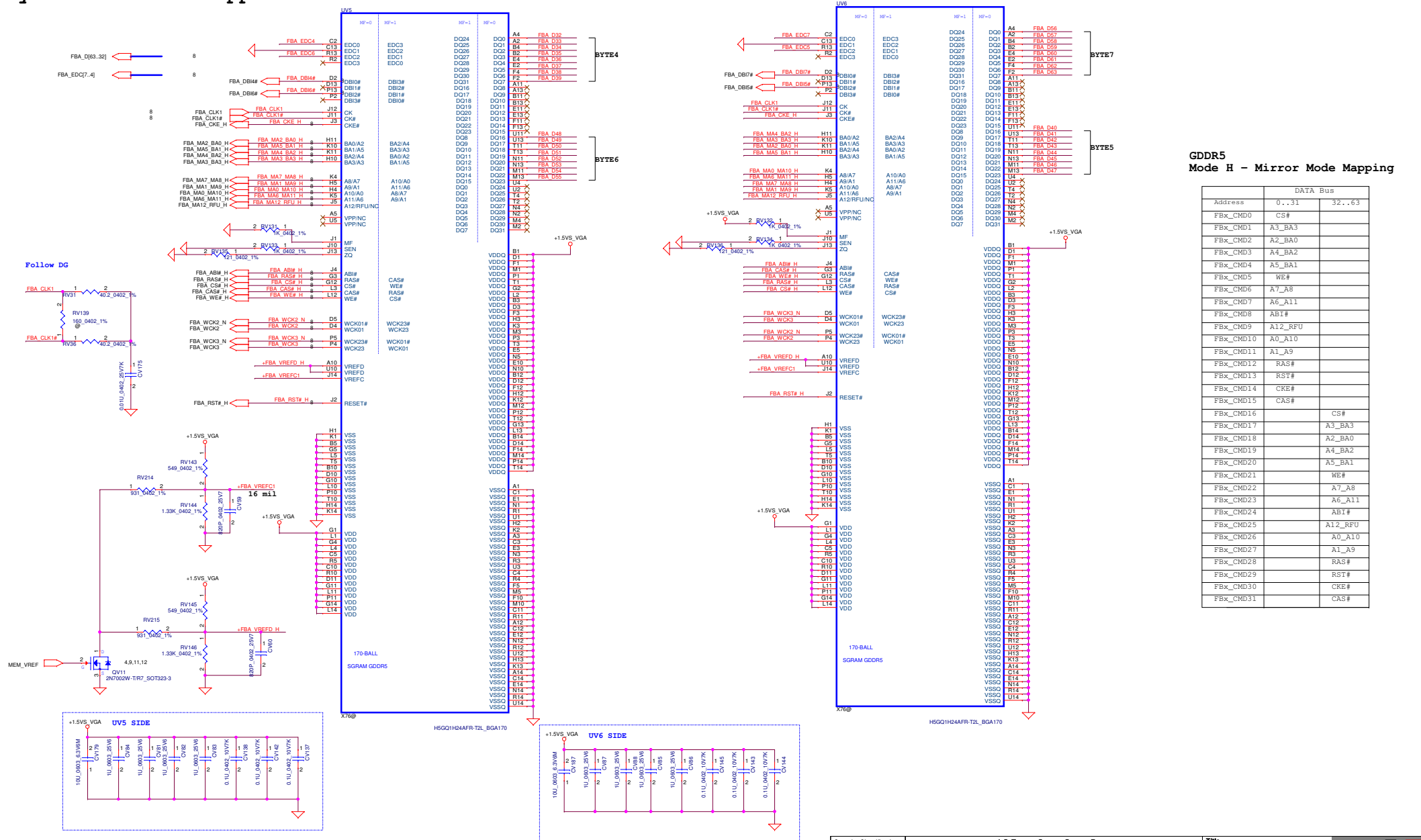
Memory Partition A - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS#	
FbX_CMD1	A3_BA3	
FbX_CMD2	A2_BA0	
FbX_CMD3	A4_BA2	
FbX_CMD4	A5_BA1	
FbX_CMD5	WE#	
FbX_CMD6	A7_A8	
FbX_CMD7	A6_A11	
FbX_CMD8	AB1#	
FbX_CMD9	A12_RFU	
FbX_CMD10	A0_A10	
FbX_CMD11	A1_A9	
FbX_CMD12	RA5#	
FbX_CMD13	RST#	
FbX_CMD14	CKE#	
FbX_CMD15	CAS#	
FbX_CMD16		CS#
FbX_CMD17		A3_BA3
FbX_CMD18		A2_BA0
FbX_CMD19		A4_BA2
FbX_CMD20		A5_BA1
FbX_CMD21		WE#
FbX_CMD22		A7_A8
FbX_CMD23		A6_A11
FbX_CMD24		AB1#
FbX_CMD25		A12_RFU
FbX_CMD26		A0_A10
FbX_CMD27		A1_A9
FbX_CMD28		RA5#
FbX_CMD29		RST#
FbX_CMD30		CKE#
FbX_CMD31		CAS#

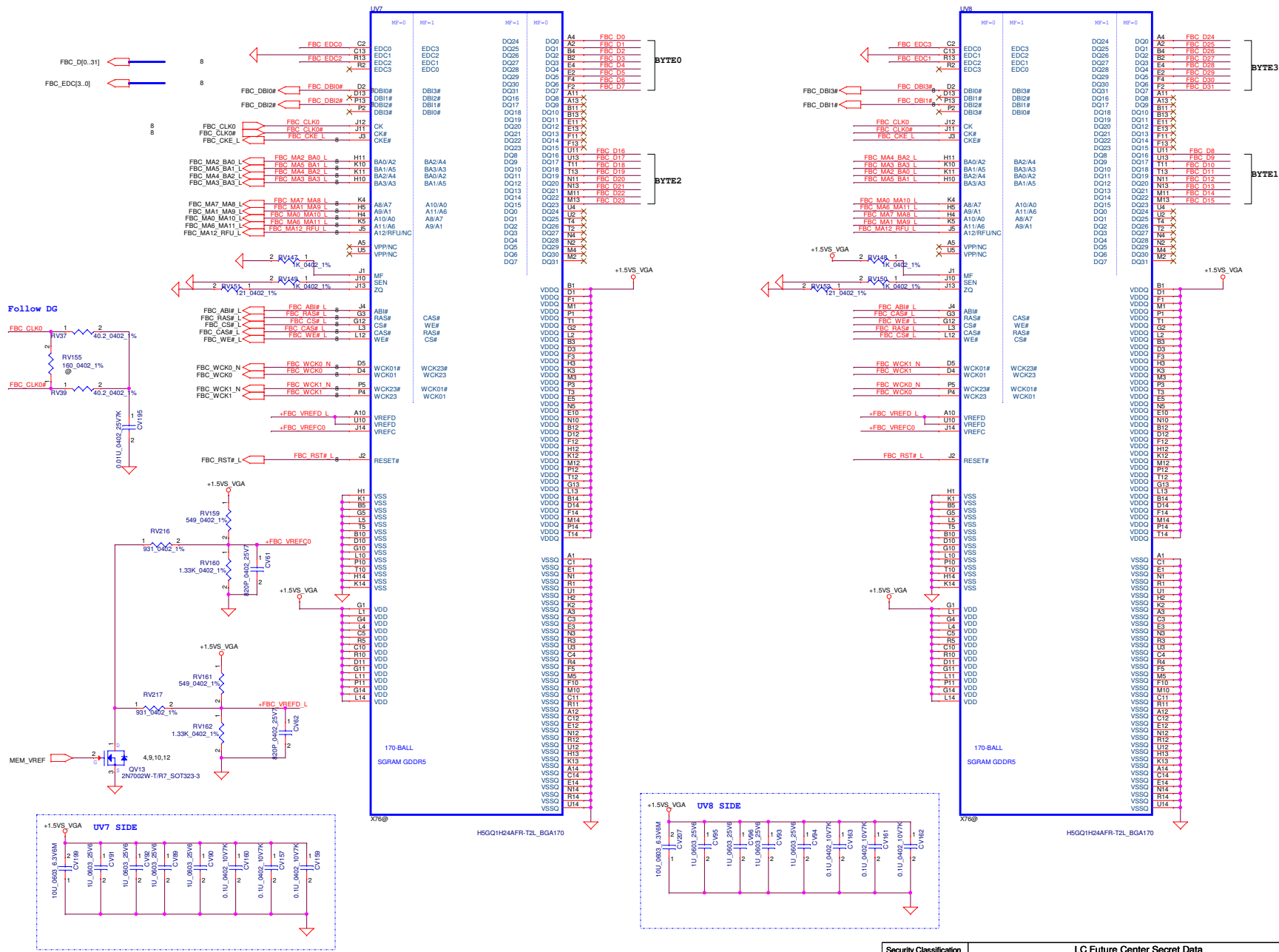
Memory Partition A - Upper 32 bits



	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS#	
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
FBX_CMD3	A4_BA2	
FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	ABI#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		ABI#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#

Security Classification	LC Future Center Secret Data			Title	
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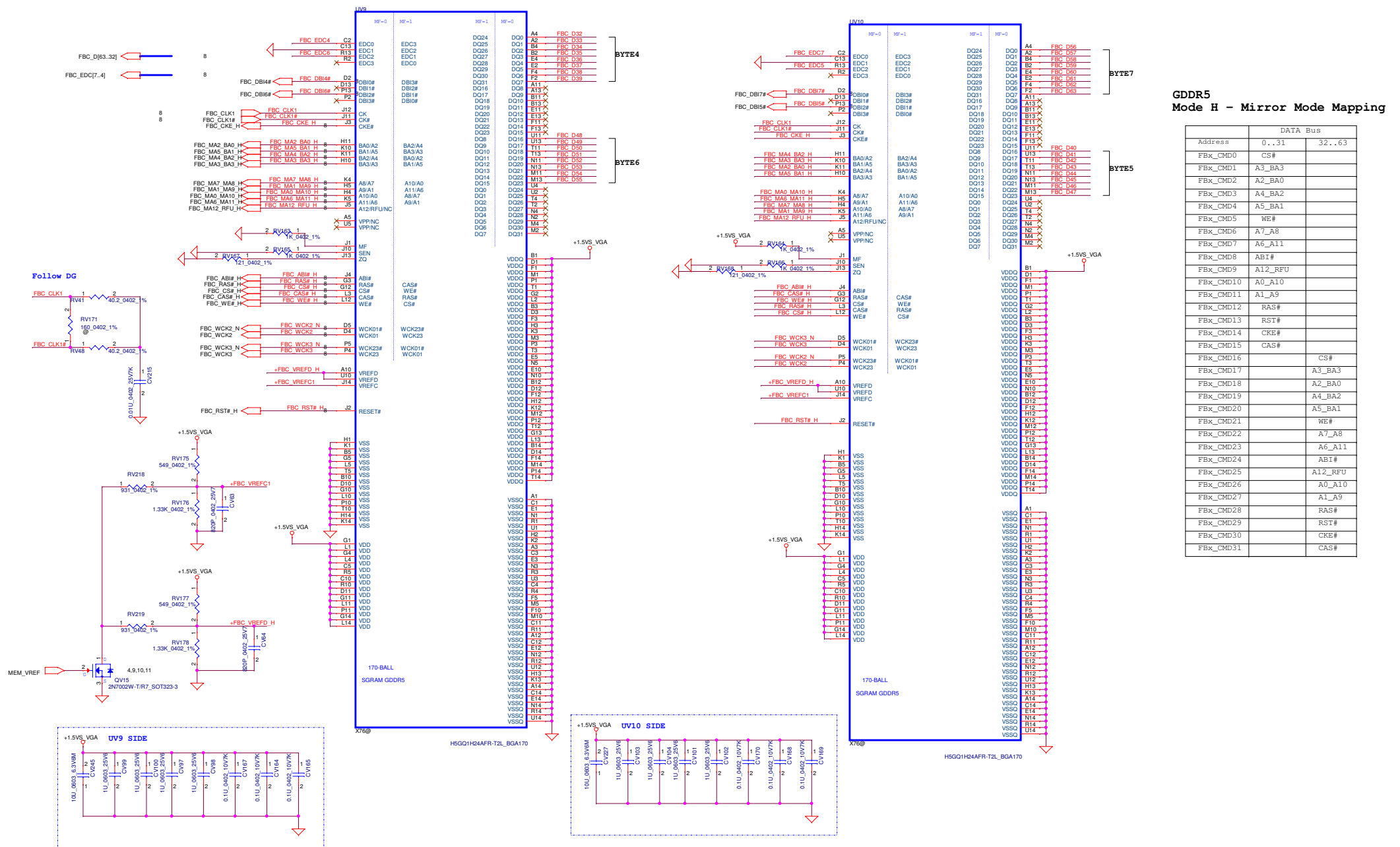
Memory Partition C - Lower 32 bits



GDDR5 Mode H - Mirror Mode Mapping

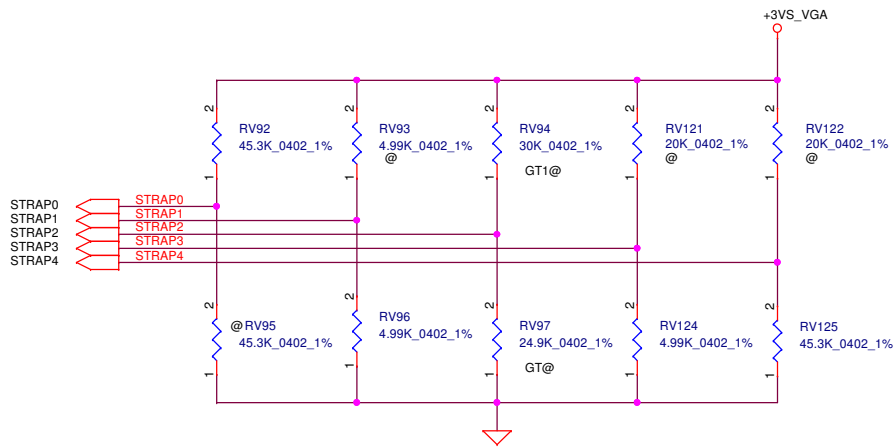
DATA Bus	
Address	0..31 32..63
FBX_CMD0	CS#
FBX_CMD1	A3_BA3
FBX_CMD2	A2_BA0
FBX_CMD3	A4_BA2
FBX_CMD4	A5_BA1
FBX_CMD5	WE#
FBX_CMD6	A7_A8
FBX_CMD7	A6_A11
FBX_CMD8	AB1#
FBX_CMD9	A12_RFU
FBX_CMD10	A0_A10
FBX_CMD11	A1_A9
FBX_CMD12	RAS#
FBX_CMD13	RST#
FBX_CMD14	CKE#
FBX_CMD15	CAS#
FBX_CMD16	
FBX_CMD17	A3_BA3
FBX_CMD18	A2_BA0
FBX_CMD19	A4_BA2
FBX_CMD20	A5_BA1
FBX_CMD21	WE#
FBX_CMD22	A7_A8
FBX_CMD23	A6_A11
FBX_CMD24	AB1#
FBX_CMD25	A12_RFU
FBX_CMD26	A0_A10
FBX_CMD27	A1_A9
FBX_CMD28	RAS#
FBX_CMD29	RST#
FBX_CMD30	CKE#
FBX_CMD31	CAS#

Memory Partition C - Upper 32 bits



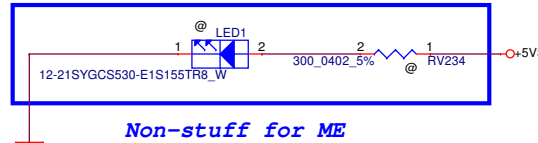
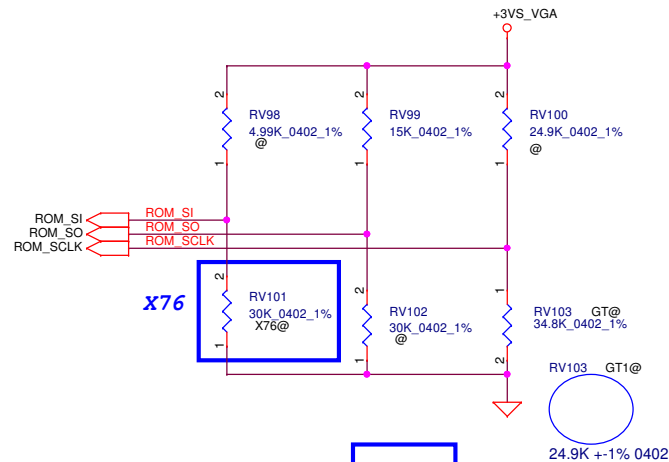
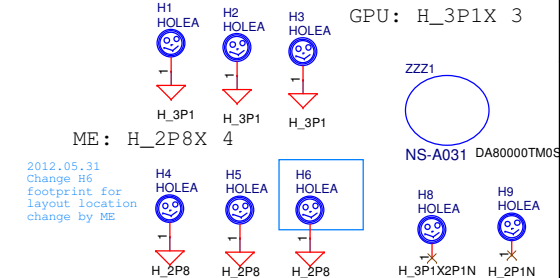
	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS#	
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
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FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	ABI#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		ABI#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

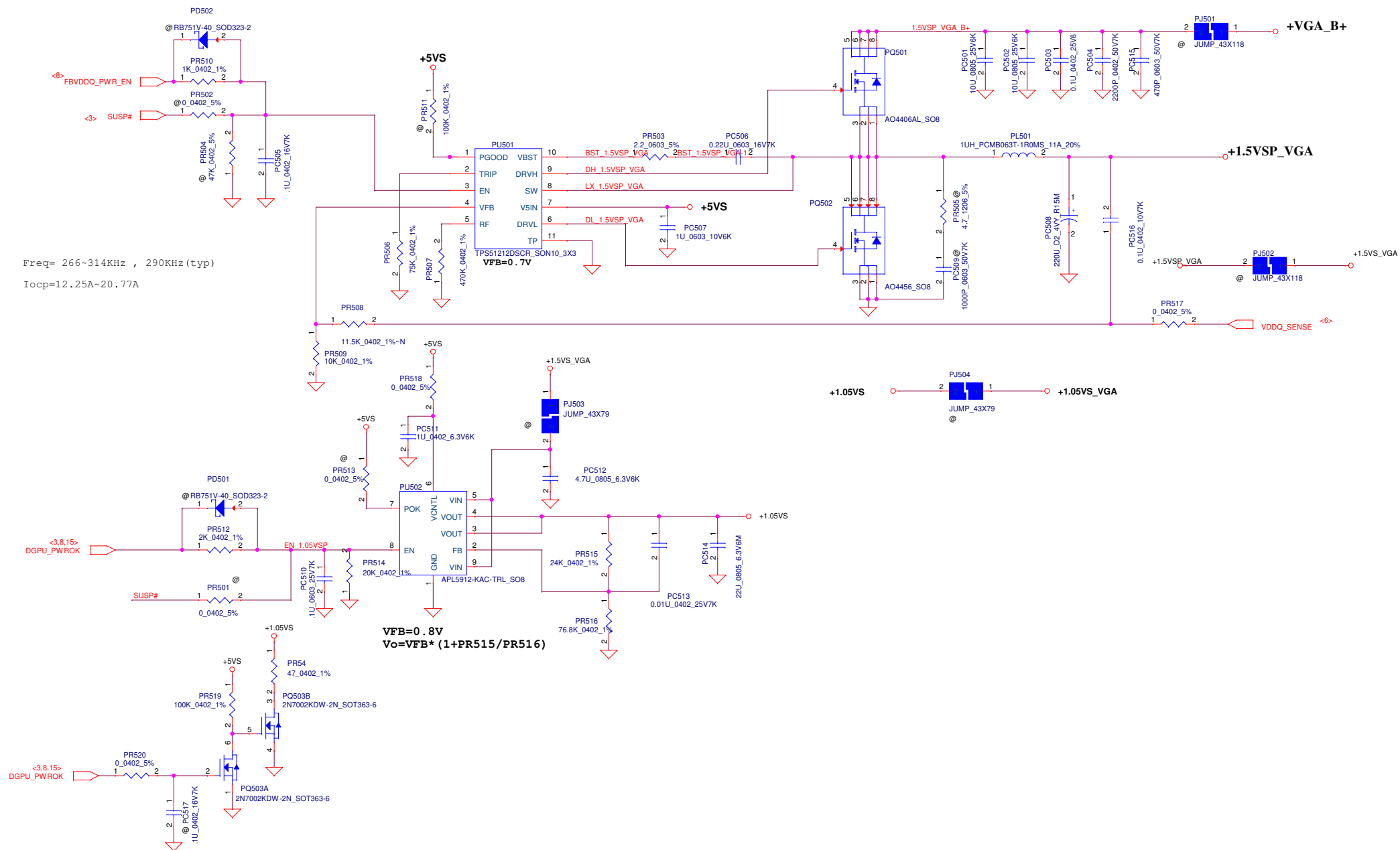
Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



3GIO_PADCFG		XCLK_417	
3GIO_PADCFG[3:0]		0	277MHz (Default)
0110	Notebook Default	1	Reserved
SLOT_CLK_CFG			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device (Class Code 302h)
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)
SUB_VENDOR		USER Straps	
0	No VBIOS ROM	User[3:0]	
1	BIOS ROM is present (Default)	1000-1100	Customer defined
FB_0_BAR_SIZE		PEX_PLL_EN_TERM	
0	Reserved	0	Disable (Default)
1	Reserved	1	Enable
2	256MB (Default)	PCIE_MAX_SPEED	
3	Reserved	0	Limit to PCIE Gen1
		1	PCIE Gen 2/3 Capable

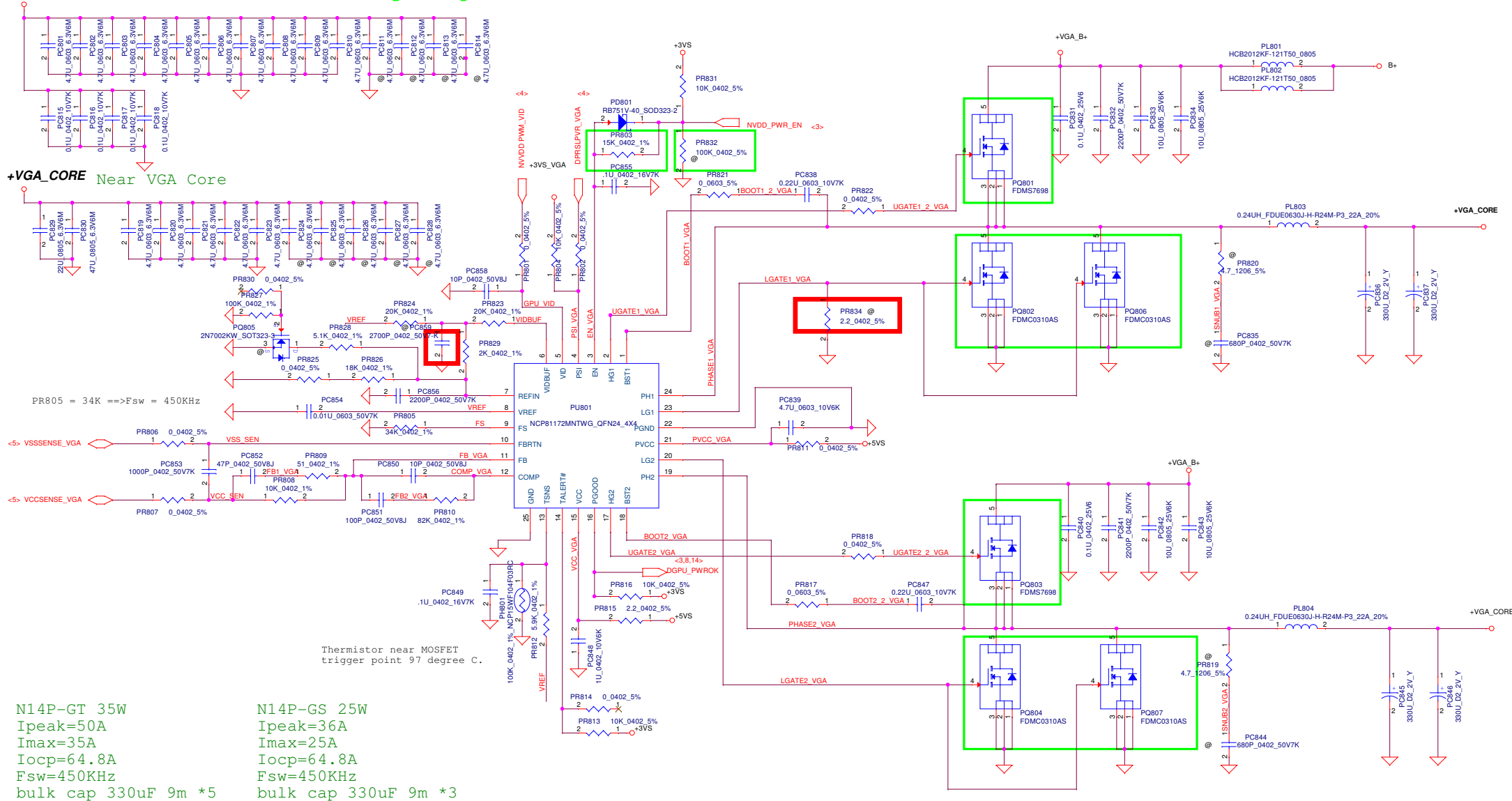
GPU		FB Memory (GDDR5)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P-GT 28nm	Samsung	K4G20325FD-FC04 2G	PD 30K	PU 15K	PD 35K	PU 45K	PD 5K	PD 25K	PD 5K	PD 45K
	Hynix	H5GQ2H24AFR-T2C 2G	PD 25K							
N14P-GT1 28nm	Samsung	K4G20325FD-FC03 2G	PD 30K	PU 15K	PD 25K	PU 45K	PD 5K	PU 30K	PD 5K	PD 45K
	Hynix	H5GQ2H24AFR-R0C 2G	PD 25K							

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+VGA_CORE Under VGA Core **GB4-128 package**

+VGA_CORE Near VGA Core



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